Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A computer system comprising:

at least one processor;

a controller for coupling said at least one processor to a peripheral bus control block and a memory module bus;

at least one peripheral bus slot coupled to said peripheral bus control block by a peripheral bus;

at least one memory module slot coupled to said memory module bus; and

a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus, wherein the processor element exchanges data at memory module bus speeds.

2. (previously presented) The computer system of claim 1 further comprising:

a control connection to said processor element coupled to said peripheral bus for indicating to said at least one processor an arrival of data on said direct data connection to said processor element and memory module bus.

3. (original) The computer system of claim 1 wherein said memory module bus comprises a DIMM bus.

4. (original) The computer system of claim 3 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.

5. (previously presented) The computer system of claim 1 wherein said memory module bus comprises a in-line memory module serial interface bus.

6. (previously presented) The computer system of claim 5 wherein said processor element comprises a in-line memory module serial interface physical format for retention within said at least one memory module slot.

7. (original) The computer system of claim 1 wherein said external device comprises one of another computer system, switch or network.

8. (original) The computer system of claim 1 wherein said peripheral bus comprises a PCI bus.

9. (original) The computer system of claim 1 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.

10. (original) The computer system of claim 1 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.

11. (original) The computer system of claim 1 wherein said processor element comprises:

a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.

12. (original) The computer system of claim 1 wherein said at least one processor comprises a plurality of processors.

13. (currently amended) A computer system comprising:

at least one processor;

a controller for coupling said at least one processor to a graphics control block and a memory module bus;

at least one graphics bus connection coupled to said graphics control block by a graphics bus;

at least one memory module slot coupled to said memory module bus; and

a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus wherein access to the processor element by the controller occurs at memory module bus speeds.

14. (previously presented) The computer system of claim 13 further comprising:

a control connection to said processor element coupled to said graphics bus for indicating to said at least one processor an arrival of data on said direct data connection to said processor element and memory module bus.

15. (original) The computer system of claim 13 wherein said memory module bus comprises a DIMM bus.

16. (original) The computer system of claim 15 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.

17. (previously presented) The computer system of claim 13 wherein said memory module bus comprises a in-line memory module serial interface bus.

18. (previously presented) The computer system of claim 17 wherein said processor element comprises a in-line memory module serial interface physical format for retention within said at least one memory module slot.

19. (original) The computer system of claim 13 wherein said external device comprises one of another computer system, switch or network.

20. (previously presented) The computer system of claim 13 wherein said graphics bus comprises an AGP bus.

21. (original) The computer system of claim 13 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.

22. (original) The computer system of claim 13 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.

23. (original) The computer system of claim 13 wherein said processor element comprises:

a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.

24. (original) The computer system of claim 13 wherein said at least one processor comprises a plurality of processors.

25. (currently amended) A computer system comprising:

at least one processor;

a controller for coupling said at least one processor to a system maintenance control block and a memory module bus;

at least one system maintenance bus connection coupled to said system maintenance control block by a system maintenance bus;

at least one memory module slot coupled to said memory module bus; and

a processor element associated with said at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus wherein access to the processor element by the controller for data exchange occurs at bus speeds substantially equal to that of the at least one microprocessor.

26. (previously presented) The computer system of claim 25 further comprising:

a control connection to said processor element coupled to said system maintenance bus for indicating to said at least one processor an arrival of data on said direct data connection to said processor element and memory module bus.

27. (original) The computer system of claim 25 wherein said memory module bus comprises a DIMM bus.

28. (original) The computer system of claim 27 wherein said processor element comprises a DIMM physical format for retention within said at least one memory module slot.

29. (previously presented) The computer system of claim 25 wherein said memory module bus comprises a in-line memory module serial interface bus.

30. (previously presented) The computer system of claim 29 wherein said processor element comprises a in-line memory module serial interface physical format for retention within said at least one memory module slot.

31. (original) The computer system of claim 25 wherein said external device comprises one of another computer system, switch or network.

32. (previously presented) The computer system of claim 25 wherein said system maintenance bus comprises an SM bus.

33. (original) The computer system of claim 25 wherein said processor element is operative to alter data received from said controller on said memory module bus prior to transmission on said data connection to said external device.

34. (original) The computer system of claim 25 wherein said processor element is operative to alter data received on said data connection from said external device prior to transmission to said controller on said memory module bus.

35. (original) The computer system of claim 25 wherein said processor element comprises:

a field programmable gate array configurable to perform an identified algorithm on an operand provided thereto on said memory module bus and said data connection.

36. (original) The computer system of claim 25 wherein said at least one processor comprises a plurality of processors.

Claims 37-51 (cancelled)